

▶ PRODUCT OVERVIEW

Marvell® Xelerated® Development Suite (XDS) provides a comprehensive environment for rapid development of wirespeed packet processing and OAM programs for Marvell Xelerated Network Processors (NPUs) and Programmable Ethernet Switches. The XDS is centered around an Integrated Development Environment, which is a graphical project oriented framework where programmers can access a full suite of tools for code editing, compilation, simulation and debugging.

Thanks to the Dataflow Architecture of Marvell Xelerated NPUs, all packets are processed with a deterministic behavior and a guaranteed number of instructions and classification lookups per packet irrespective of traffic patterns, protocols used and packet sizes. The architecture inherently brings a linear single-threaded programming model, where the programmer does not need to deal with complex tasks such as processor load balancing, packet ordering, and synchronization of common resources. This eliminates the need for time-consuming performance optimization and allows the programmer to focus on the most important task when developing data plane software: systemization and code implementation. The result is significantly shorter time to market with highly efficient, high quality data plane software.

▶ NETWORK PROCESSOR CODE DEVELOPMENT

The XDS consists of tools and support functions for developing and integrating high performance code for the network processor. The functions are used to develop code both for forwarding and OAM functions.

▶ POWERFUL SIMULATOR, TIGHT INTEGRATION

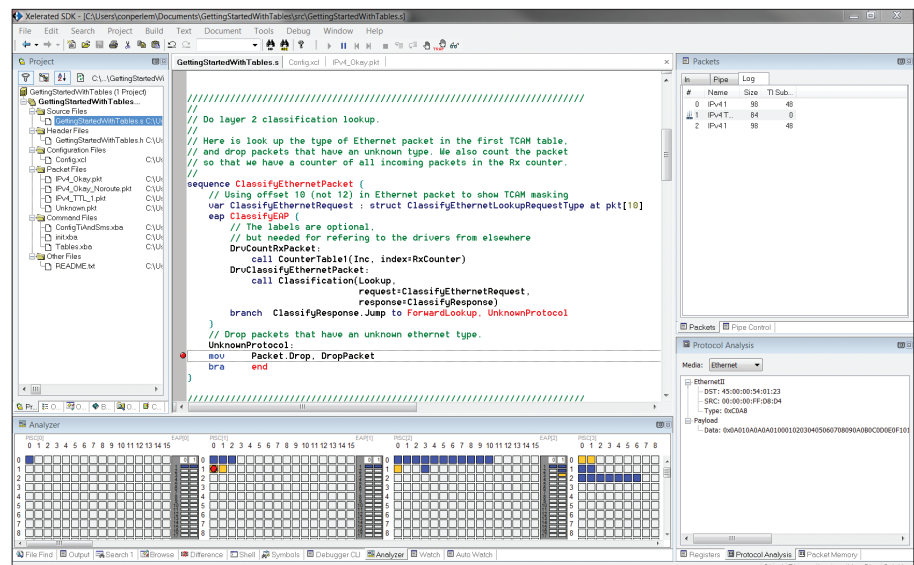
The simulator is a software model of the network processor focused at functional simulation of the Programmable Pipeline and the Engines of the NPUs. Simulation is clock-cycle correct, and the traffic interfaces are also represented to simulate different traffic paths through the device. The simulator has a powerful debugger which aids in the development of data plane software. It is used both in the early phases of development, before line cards are available, and throughout the whole development cycle, including the test phases of the hardware.

It is easy and intuitive to set breakpoints, trace the execution of the code and inspect the execution context of a packet at any processor stage in the Programmable Pipeline. If the simulator is connected to a hardware target through the Hardware Target Connection Agent, the code can be debugged in hardware directly from the IDE by setting traps in the code. Packets can be trapped in hardware and exported into the simulator for further analysis or continued single step execution.

The simulator can also be used together with control-plane software for control plane co-simulation over socket interfaces.

The IDE integrates the simulator and the other tools of the XDS into a complete framework for developing data plane software. The developer gains access to all the memories and registers of the simulator or hardware target with ability to set watches and do advanced packet-based protocol analysis.

Source code debugging is performed by injecting packets into the Programmable Pipeline from the IDE or from a scripted regression test suite. As the packet, by classifications and packet processing, executes its program it can be fully controlled and all the attributes of the packet program can be monitored.

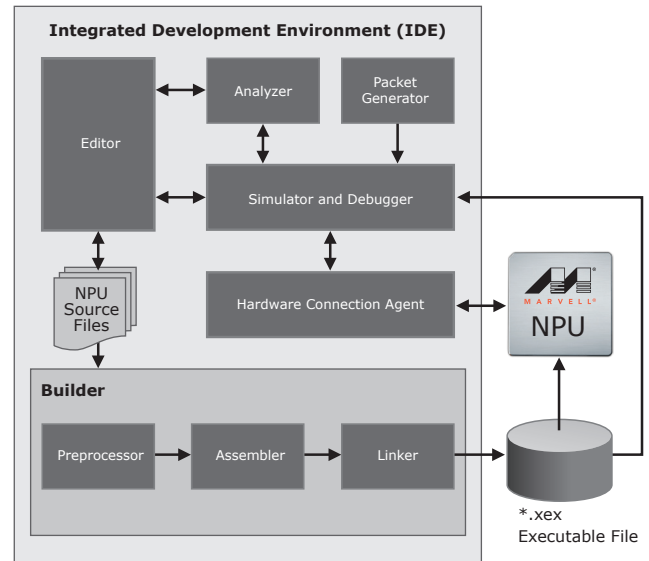


Xelerated Development Suite features a highly Integrated Development Environment from where all tools can be accessed.

Marvell Xelerated Development Suite (XDS)

OVERVIEW OF TOOLS

IDE (Integrated Development Environment)	Project oriented graphical environment that integrates all the tools needed for development of data plane software.
Source Code Editor	Multi-tabbed, color coded editor with advanced browsing capabilities. Integrated with Simulator for symbolic source code debugging.
Builder	Pre-processor, assembler and linker for NPU code. Can be used within the IDE or as stand-alone scriptable CLI tools for automated build environments.
Analyzer	Provides a graphical overview of how the code is mapped onto the packet processing elements of the NPU.
Simulator and Debugger	Clock cycle correct model of the packet processing elements of the NPU that allows single stepping, breakpoints and watches.
Hardware Target Connection Agent	Agent for connection to target hardware over a standard TCP/IP socket connection. Allows hardware debugging directly from the IDE.
Packet Generator	Creates test packet with a library of standard headers or with fully customized headers and content.
Get Started Data Plane Software	Basic forwarding plane code for evaluation and education purposes.



KEY FEATURES AND BENEFITS

SPECIAL FEATURES

- Project oriented graphical IDE
- Common environment across NPU product line
- XPL Xelerated Programming Language
- ANSI-C data structures
- Auto-allocation of variables to registers
- Clock cycle accurate simulator
- Performance guaranteed
- TCP/IP-based target hardware connection
- In-service debugging
- Integrated code coverage tool
- Graphical code analyzer
- Scriptable Build Suite over CLI

BENEFITS

- Keeps all files associated with the data plane software organized and gives intuitive access to all tools for data plane development.
- Speeds up development, encourages code co-use, and simplifies migration between use of X11, HX and AX for different target systems.
- Easy to learn and efficient packet optimized language.
- Simplifies system integration by allowing for sharing of data structures between control and data planes.
- High abstraction level; the programmer does not need to deal with exact location of data during the program development.
- Shortens time-to-market by enabling early development of NPU software. Also reduces need for allocating hardware to software design teams.
- Marvell Xelerated NPUs give deterministic packet processing performance without need for time-consuming performance optimization tools.
- Allows connection over the company network to e.g. a lab with target hardware for testing code remotely.
- Inject, capture packets and set breakpoints in live running systems without affecting other traffic. Improves system availability for the end customer.
- Improves quality in testing by analyzing and highlighting used/unused code and functions.
- Overview of all used resources in the NPU and helps to optimize resource usage by visualizing how internal resources are used.
- Full control over the build process and integration into automated build suites.

THE MARVELL ADVANTAGE: Marvell chipsets come with complete reference designs which include board layout designs, software, manufacturing diagnostic tools, documentation, and other items to assist customers with product evaluation and production. Marvell's worldwide field application engineers collaborate closely with end customers to develop and deliver new leading-edge products for quick time-to-market. Marvell utilizes world-leading semiconductor foundry and packaging services to reliably deliver high-volume and low-cost total solutions.

ABOUT MARVELL: Marvell is a leader in storage, communications, and consumer silicon solutions. Marvell's diverse product portfolio includes switching, transceiver, communications controller, processor, wireless, power management, and storage solutions that power the entire communications infrastructure, including enterprise, metro, home, storage, and digital entertainment solutions. For more information, visit our Web site at www.marvell.com.



Marvell Semiconductor, Inc.
5488 Marvell Lane
Santa Clara, CA 95054
Phone 408.222.2500
www.marvell.com

Copyright © 2012. Marvell International Ltd. All rights reserved. Marvell, the Marvell logo, Xelerated and PISC are registered trademarks of Marvell. All other trademarks are the property of their respective owners.

Marvell_XDS-001 04/12